In the Specification:

Please amend paragraph 0023 as follows:

Figs. 4A through 4E [[4B]] illustrate steps of a known process for fabricating memory cells and arrays.

Please amend paragraph 0027 as follows:

Figs. 8A [[8a]] through 8B [[8C]] are cross-sectional views showing process steps in accordance with the invention.

Please amend paragraph 0073 as follows:

When the device is fabricated without an etch-stop layer, a timed etching step is carried out so that most or all of the TEOS layer is removed without removing any insulator material that is present below the depth of the bottom of the M0 metal layer, as Fig. 9 [[9A]] shows. Alternatively, when an etch-stop layer 90 is present, the etch-back process is carried out until the etch-stop layer 90 is reached, as Fig. 10 [[9B]] shows.